

- [c8] The integrated circuit of claim 5 wherein an active test signal is provided at either the first or second test input terminal to increase the magnitude of the first or second read signal.
- [c9] The integrated circuit of claim 8 wherein the magnitude of the read signal equal at V_{LO} is increased to reduce the differential read signal.
- [c10] The integrated circuit of claim 9 wherein the magnitude of V_{LO} is increased to V_{LOTest} , where V_{LOTest} is between V_{LO} and V_{HI} .
- [c11] The integrated circuit of claim 9 wherein the magnitude of V_{LO} is increased to V_{LOTest} , where V_{LOTest} is equal to about half way between V_{LO} and V_{HI} .
- [c12] The integrated circuit of claim 9 wherein the magnitude of V_{LO} is increased to V_{LOTest} , where V_{LOTest} is equal to about one third between V_{LO} and V_{HI} .
- [c13] The integrated circuit of claim 9 wherein the increase in magnitude of the read signal depends on the capacitance of the test capacitor and magnitude of the active test signal.
- [c14] The integrated circuit of claim 13 wherein the magnitude of V_{LO} is increased to V_{LOTest} , where V_{LOTest} is between V_{LO} and V_{HI} .
- [c15] The integrated circuit of claim 13 wherein the magnitude of V_{LO} is increased to V_{LOTest} , where V_{LOTest} is equal to about half way between V_{LO} and V_{HI} .
- [c16] The integrated circuit of claim 13 wherein the magnitude of V_{LO} is increased to V_{LOTest} , where V_{LOTest} is equal to about one third between V_{LO} and V_{HI} .
- [c17] The integrated circuit of claim 4 wherein the test circuit comprises:
a first set of x test capacitors having first terminals coupled to respective first input test signals and the second terminals coupled to the first bitline; and
a second set of y test capacitors having first terminals coupled to respective second input test signals and second terminals coupled to the second bitline.
- [c18] The integrated circuit of claim 17 wherein the capacitors within the first set have different values and the capacitors within the second set have different values.

- [c19] The integrated circuit of claim 18 wherein first set of test capacitors can vary the first read signal by $2^x - 1$ levels and the second set of test capacitors can vary the read signal by $2^y - 1$ levels.
- [c20] The integrated circuit 19 of claim wherein $x = y$.